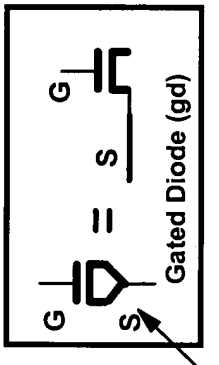

G
S
G
S
Gated Diode (gd)
190

FIG. 1A

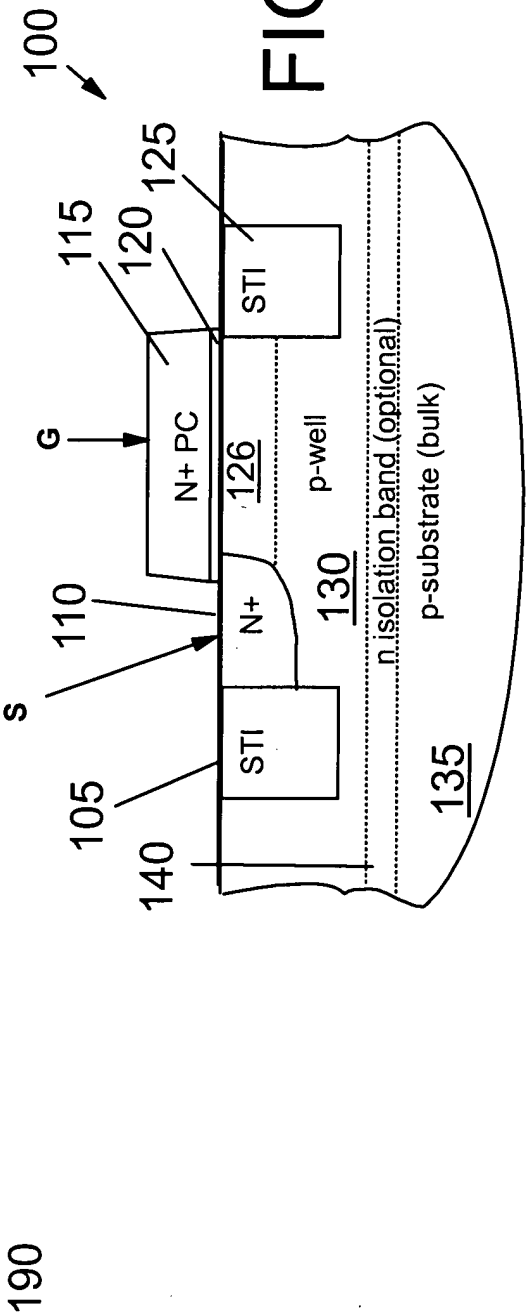

100
125
115
120
G
N+ PC
126
STI
p-well
110
S
N+
130
n isolation band (optional)
p-substrate (bulk)
105
STI
135
140

FIG. 1B

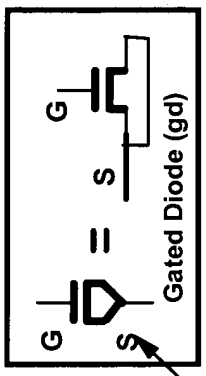

G
S
=
G
S
Gated Diode (gd)

FIG. 2A

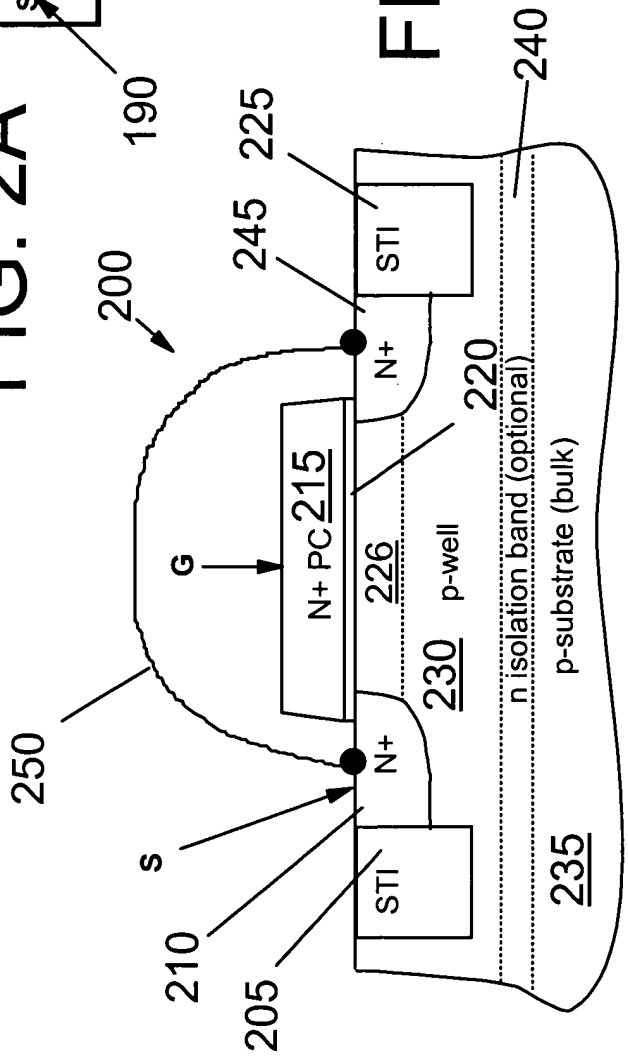

190
200
225
245
240
STI
N+
220
G
N+ PC 215
226
p-well
230
n isolation band (optional)
p-substrate (bulk)
250
S
210
205
STI
235

FIG. 2B

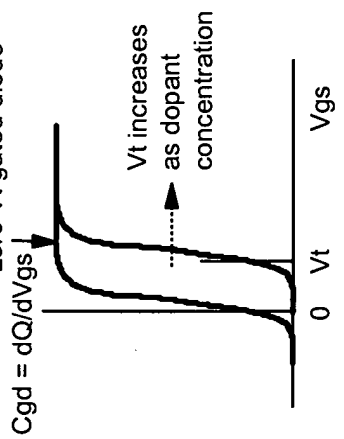

zero Vt gated diode
Cgd = dQ/dVgs
Vt increases
as dopant
concentration
0 Vt
Vgs

FIG. 3A

YOR920030604US1

Gated Diode Capacitance vs Gate-to-Source Voltage (Vgs)
Each curve represents a different gated diode gate size.
threshold voltage = 0.2 V

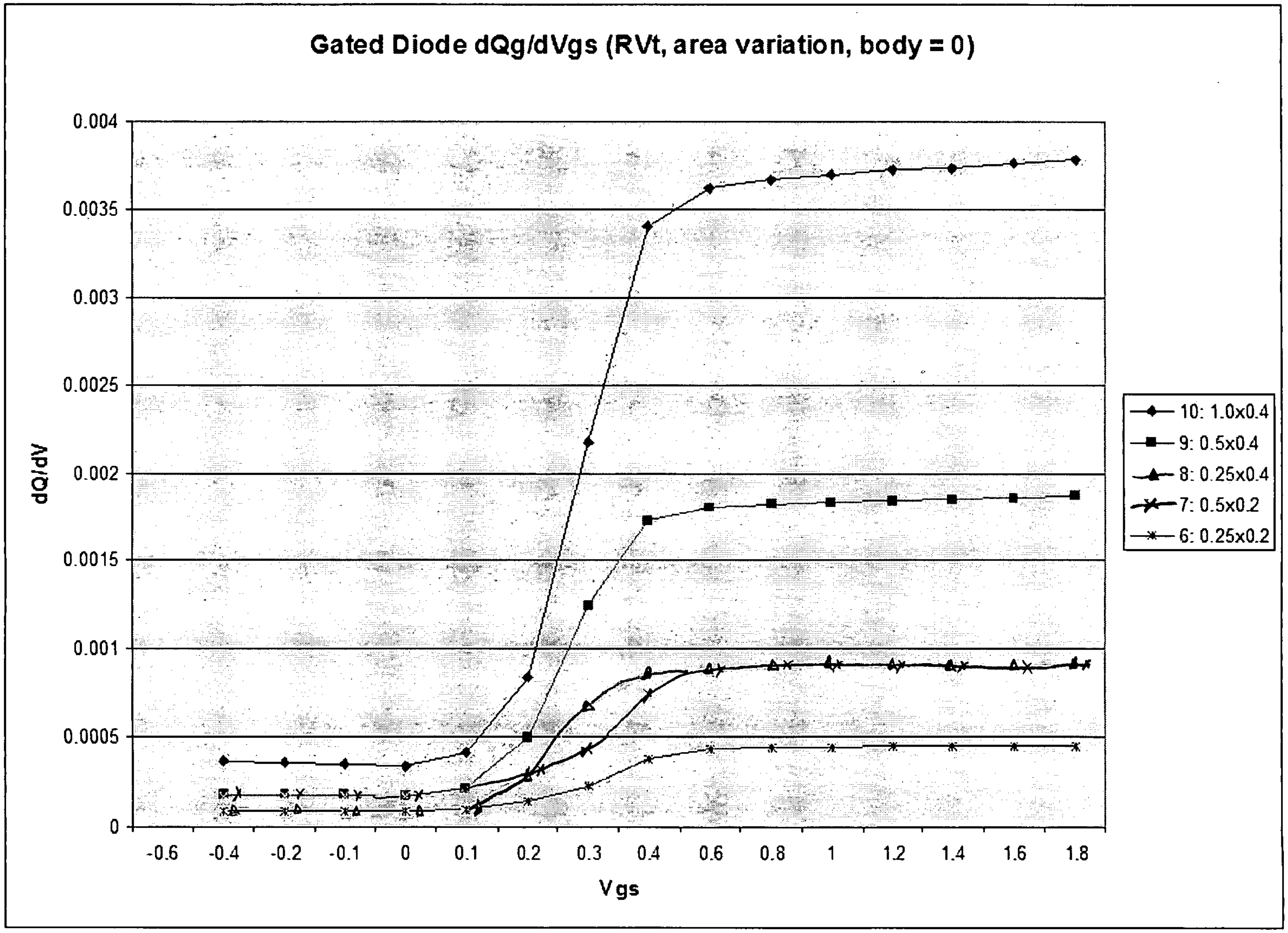
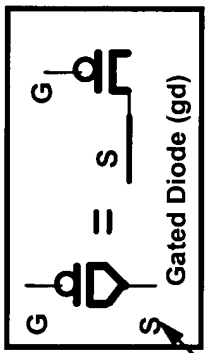


FIG. 3B



490

FIG. 4A

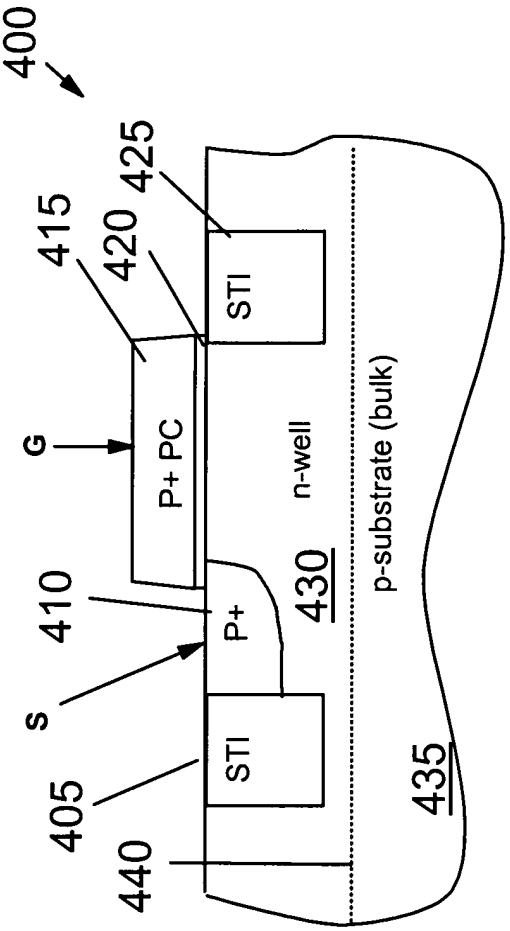


FIG. 4B

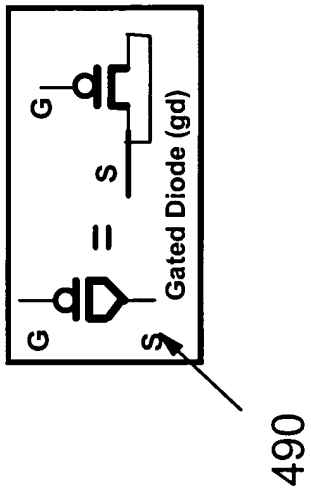

G
S
=
G
S
Gated Diode (gd)
490

FIG. 5A

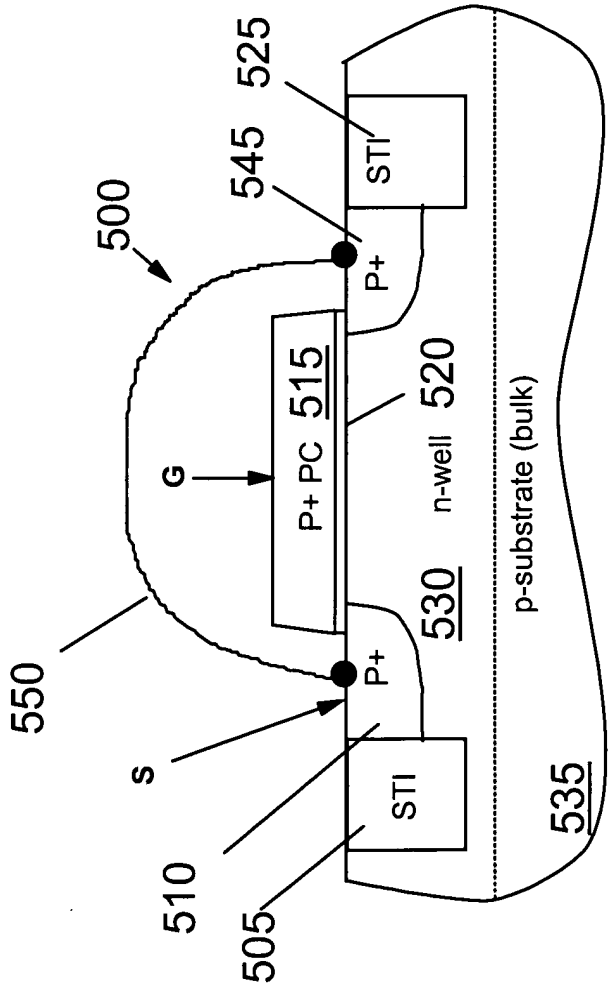

500
525
545
STI
P+
P+ PC 515
520
n-well
G
530
P+
STI
p-substrate (bulk)
535
550
S
510
505

FIG. 5B

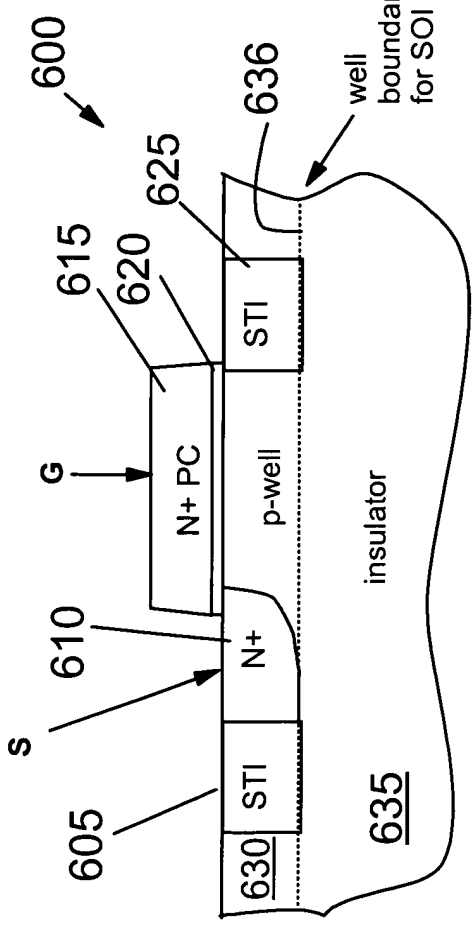

600
615
620
625
636
well boundary for SOI
G
N+ PC
p-well
STI
610
N+
insulator
S
605
STI
630
635

FIG. 6

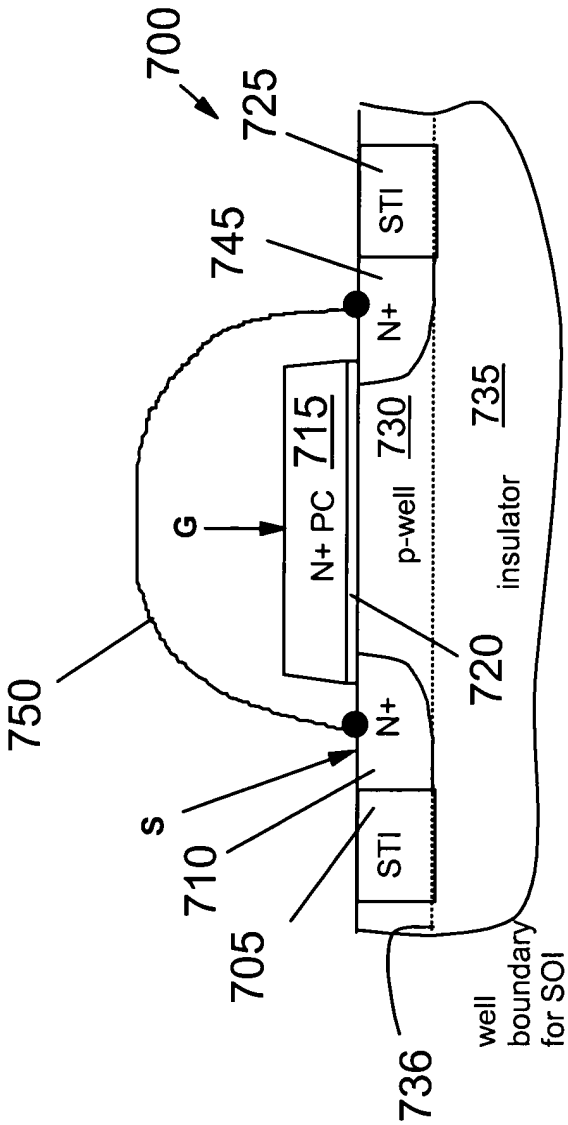

700
725
745
STI
N+
G
N+ PC 715
p-well 730
735
insulator
750
720
N+
S
710
STI
705
736
well boundary for SOI

FIG. 7

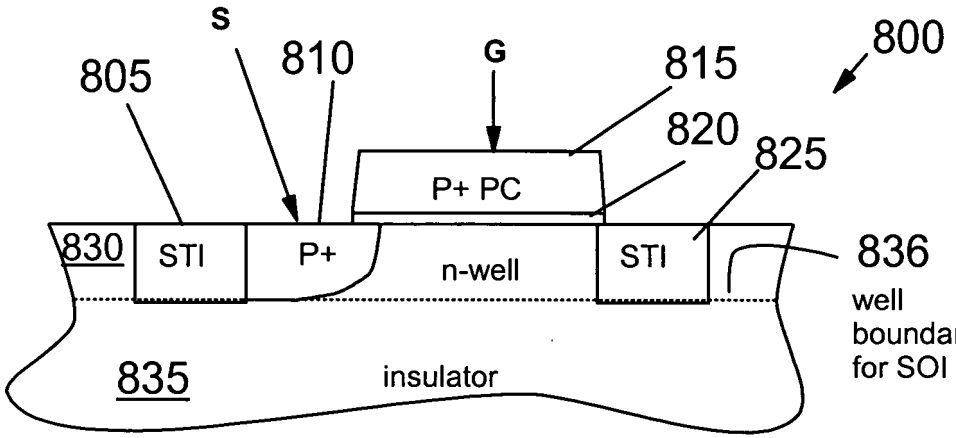


FIG. 8

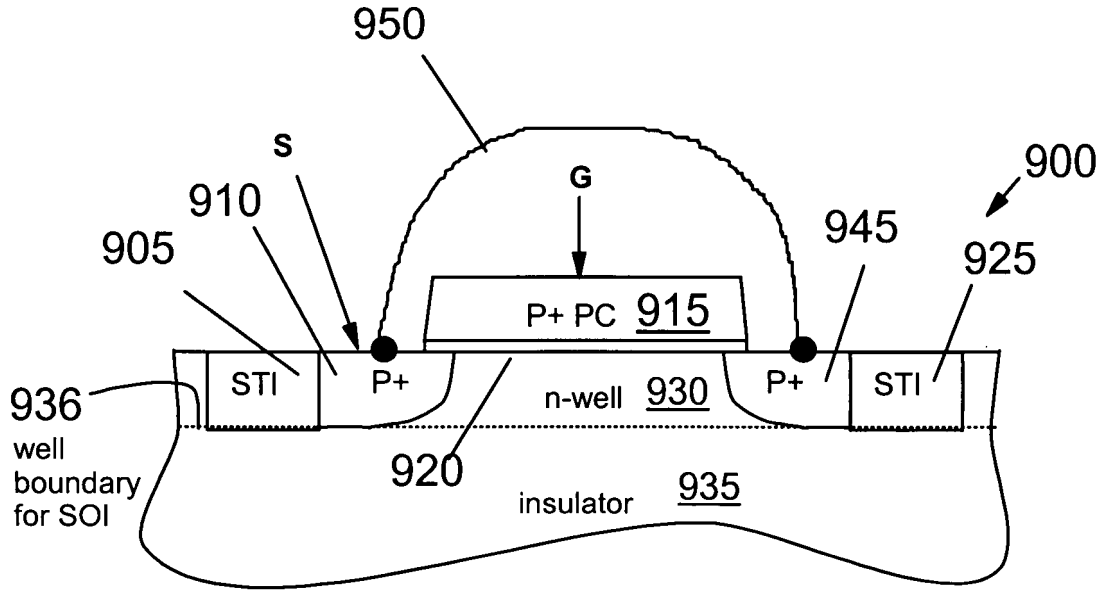
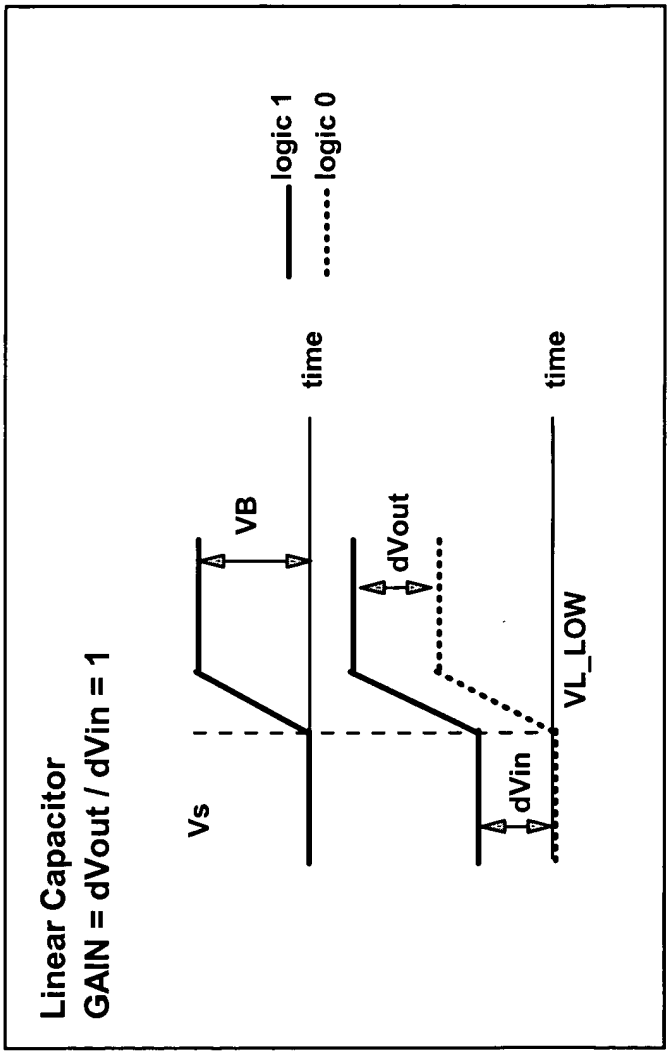


FIG. 9

FIG. 10


Linear Capacitor
GAIN = dVout / dVin = 1
Vs
VB
time
logic 1
logic 0
dVout
dVin
VL_LOW
time

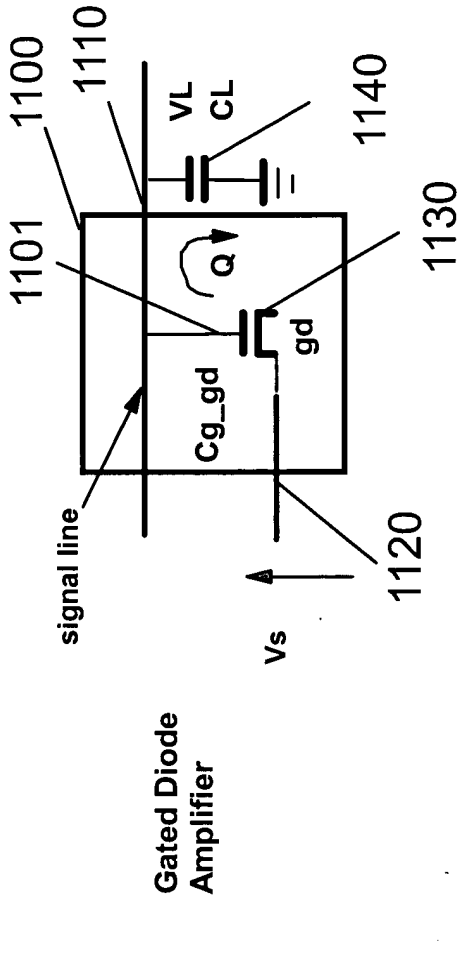


FIG. 11A

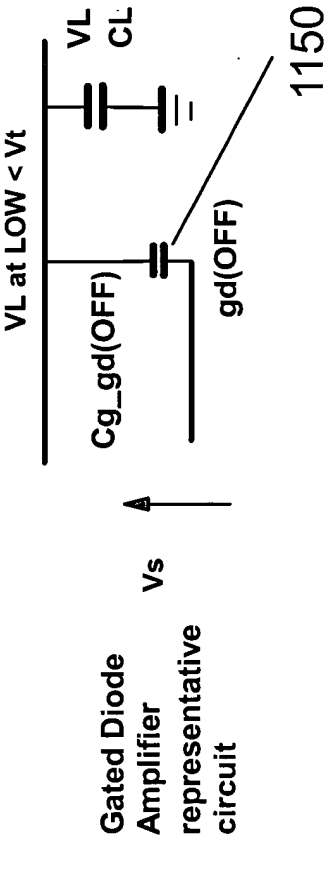


FIG. 11B

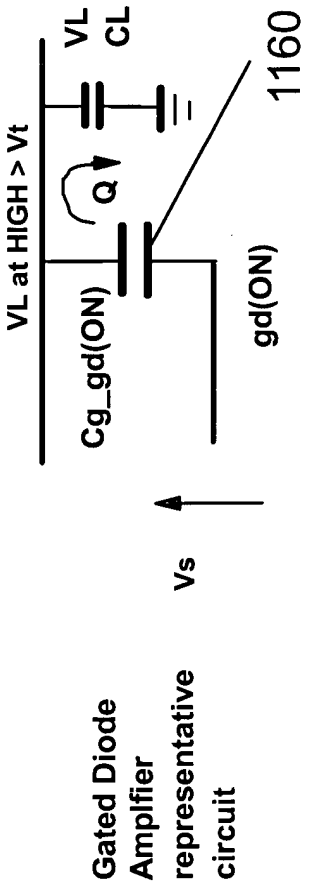


FIG. 11C

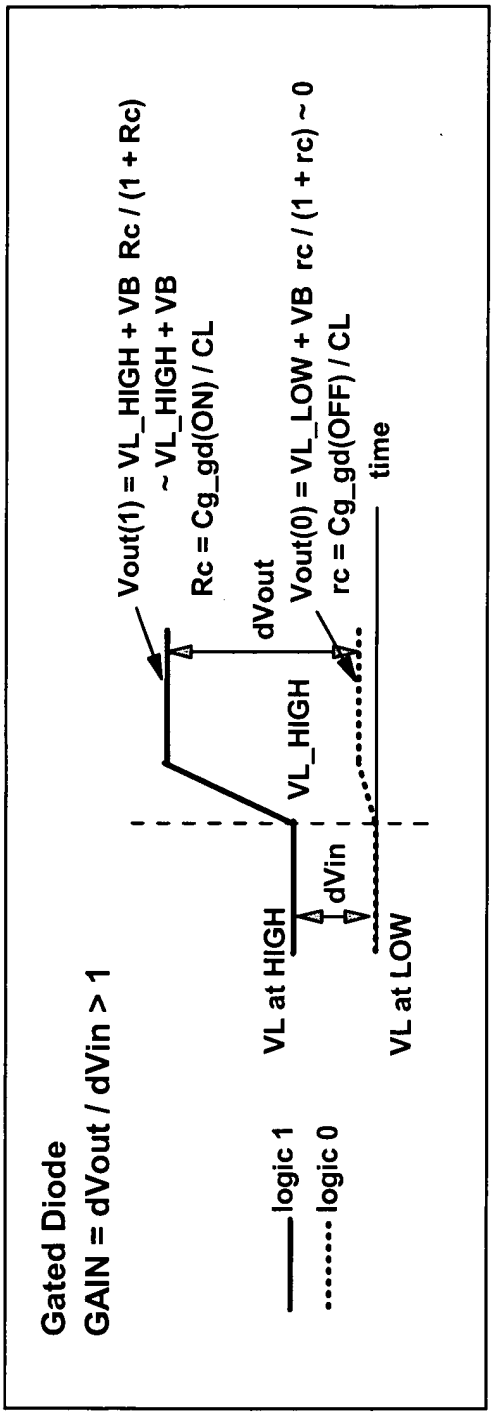


FIG. 12A

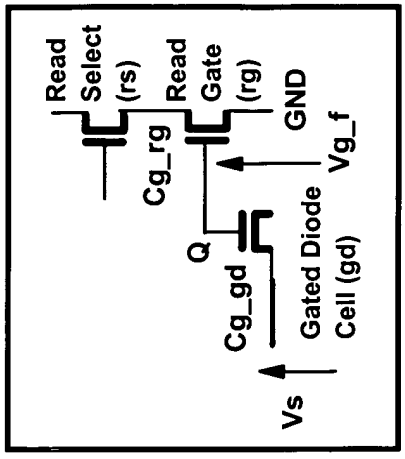


FIG. 12B

Rc = Cg_gd / Cg_rg
Gain = Vg_f / Vg_i

Gain = 1 + Rc - (Vt_gd / Vg_i) Rc ~ 1 + Rc complete charge transfer (for small Rc)
Gain = (1 + Vs / Vg_i) Rc / (1 + Rc) constrained charge transfer (large Rc)

Vg_i = 0.4 V, Vt_gd = 0

exemplary operating point

Cg_gd / Cg_rg	0.01	0.1	1	2	5	10	100	
1 + Rc	1.01	1.1	2	3	6	11	101	
Rc / (1 + Rc)	0.01	0.09	0.5	0.67	0.83	0.91	0.99	
(1+Vs/Vg_i)Rc/(1+Rc)	0.035	0.32	1.75	2.35	2.91	3.19	3.47	Vs / Vg = 2.5
(1+Vs/Vg_i)Rc/(1+Rc)	0.04	0.36	2.00	2.68	3.32	3.64	3.96	Vs / Vg = 3
Gain	1.01	1.1	2	2.68	3.32	3.64	3.96	Vs / Vg = 3
Charge Transfer	<---	complete	--->	<---	constrainted	--->		

FIG. 12C

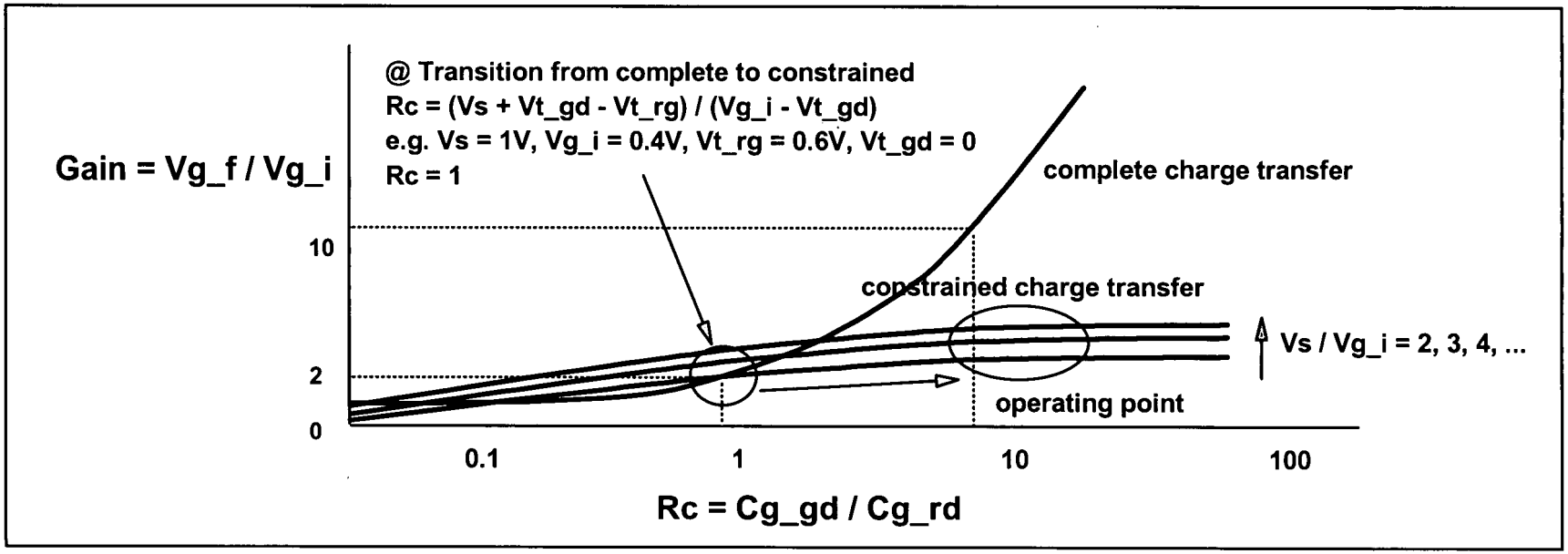


FIG. 12D

WO2003060951

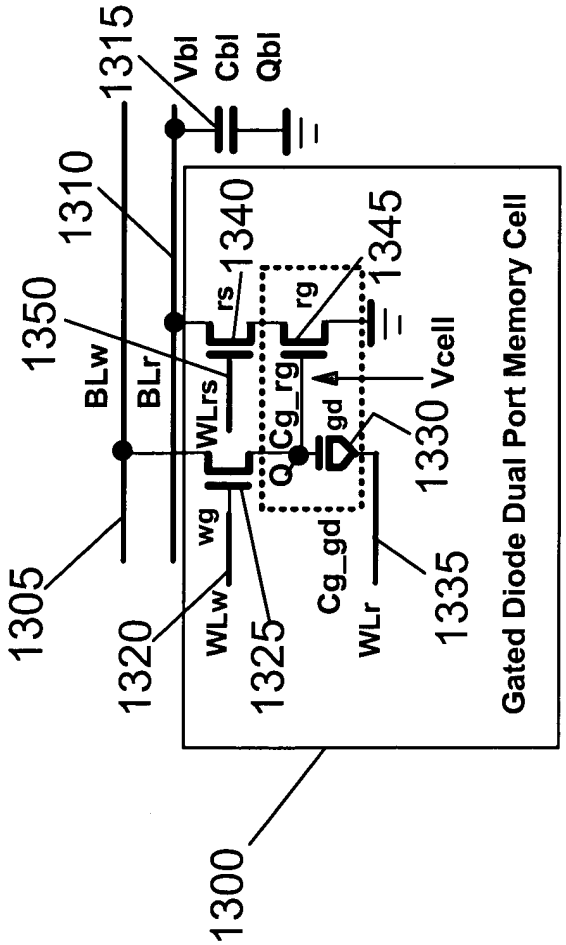


FIG. 13

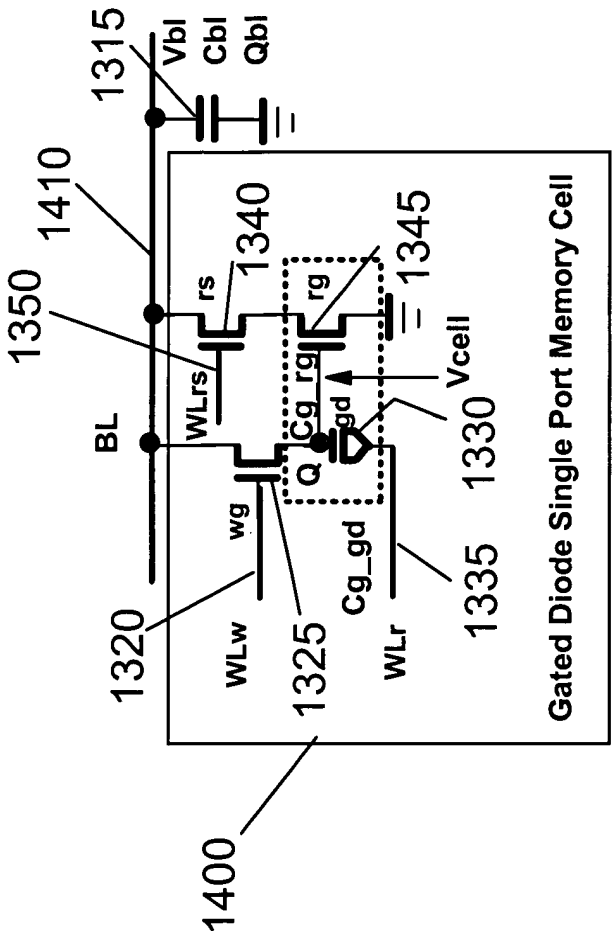

1315
Vbl
Cbl
Qbl
1410
1350
1340
1345
rs
rg
WLrs
Cg_rg
gd
Vcell
BL
Q
1330
wg
Cg_gd
1335
1320
WLw
1325
WLr
Gated Diode Single Port Memory Cell
1400

FIG. 14

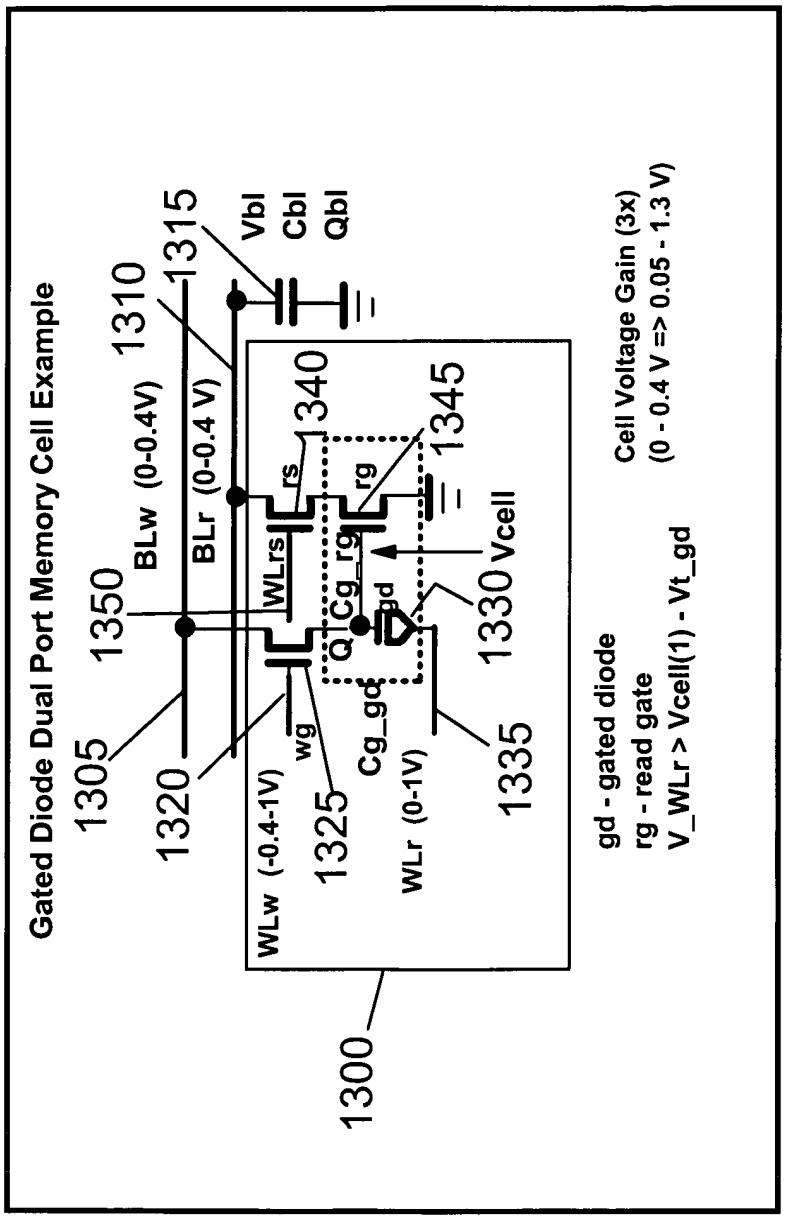

Gated Diode Dual Port Memory Cell Example
1305
1350
BLw (0-0.4V)
1310
1315
Vbl
Cbl
Qbl
1320
BLr (0-0.4 V)
WLrs
rs
1340
rg
1345
Cg_rg
Q
Cg_gd
gd
Vcell
1330
wg
WLw (-0.4-1V)
1325
WLr (0-1V)
1335
1300
gd - gated diode
rg - read gate
V_WLr > Vcell(1) - Vt_gd
Cell Voltage Gain (3x)
(0 - 0.4 V => 0.05 - 1.3 V)

FIG. 15

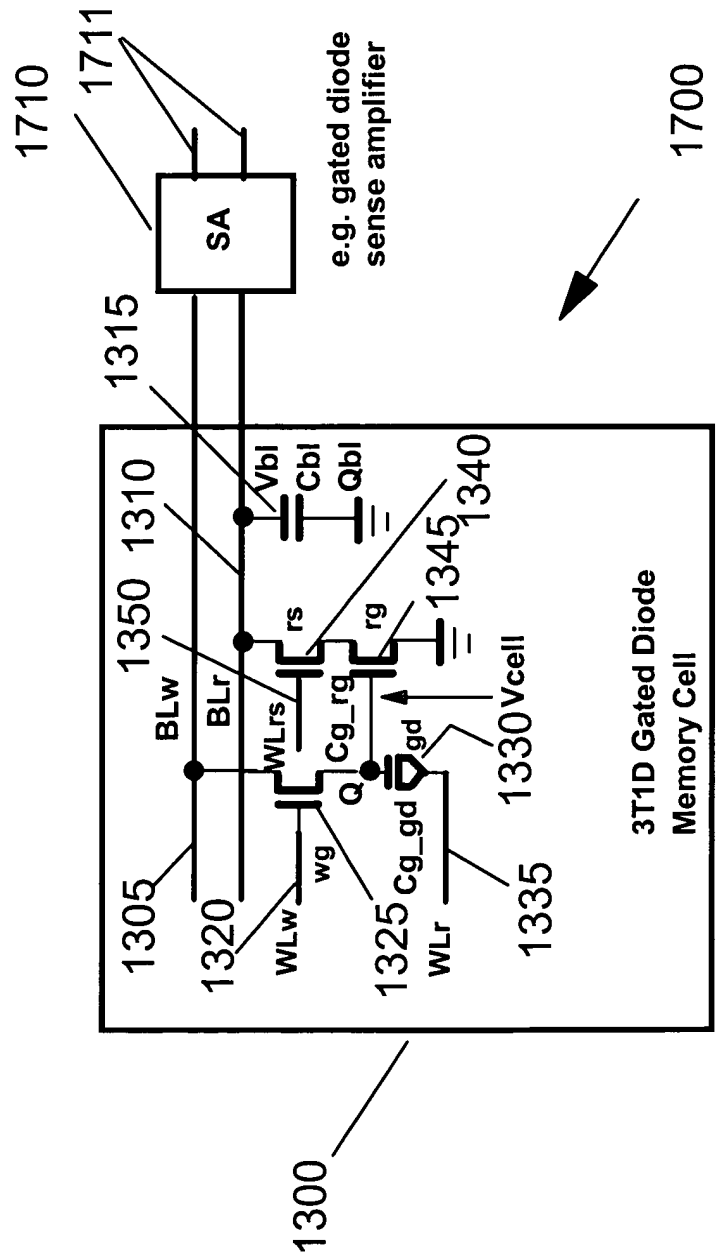

1710
1711
SA
e.g. gated diode
sense amplifier
1700
1315
1310
1350
1340
1345
1330
1305
1320
1325
1335
1300
BLw
BLr
WLrs
WLw
wg
WLr
Vbl
Cbl
Qbl
rs
rg
Cg_rg
Cg_gd
gd
Q
Vcell
3T1D Gated Diode
Memory Cell

FIG. 16

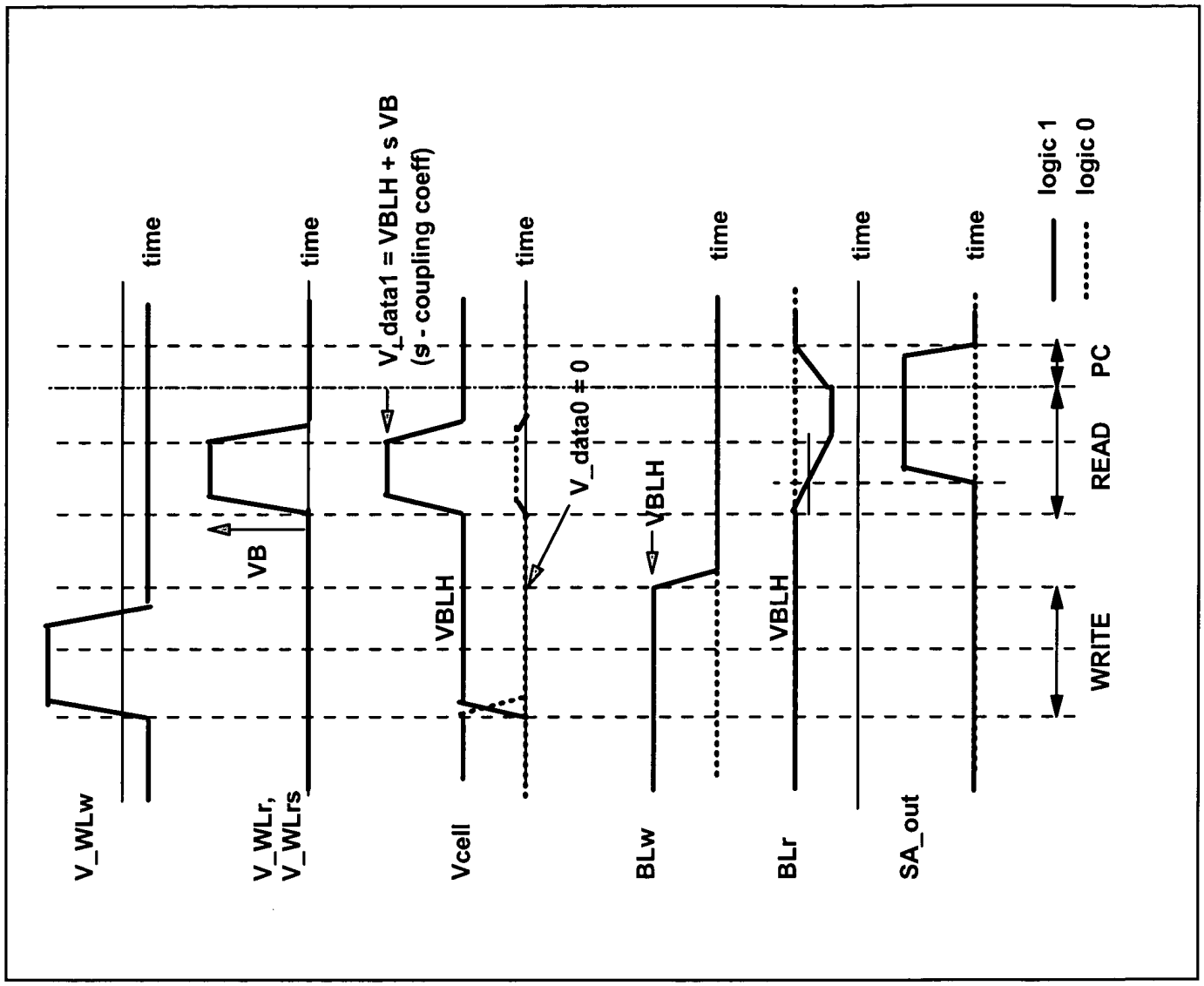

V_WLw
V_WLr,
V_WLrs
Vcell
BLw
BLr
SA_out
time
VB
VBLH
V_data1 = VBLH + s VB
(s - coupling coeff)
V_data0 ≠ 0
VBLH
VBLH
logic 1
logic 0
READ
PC
WRITE

FIG. 17

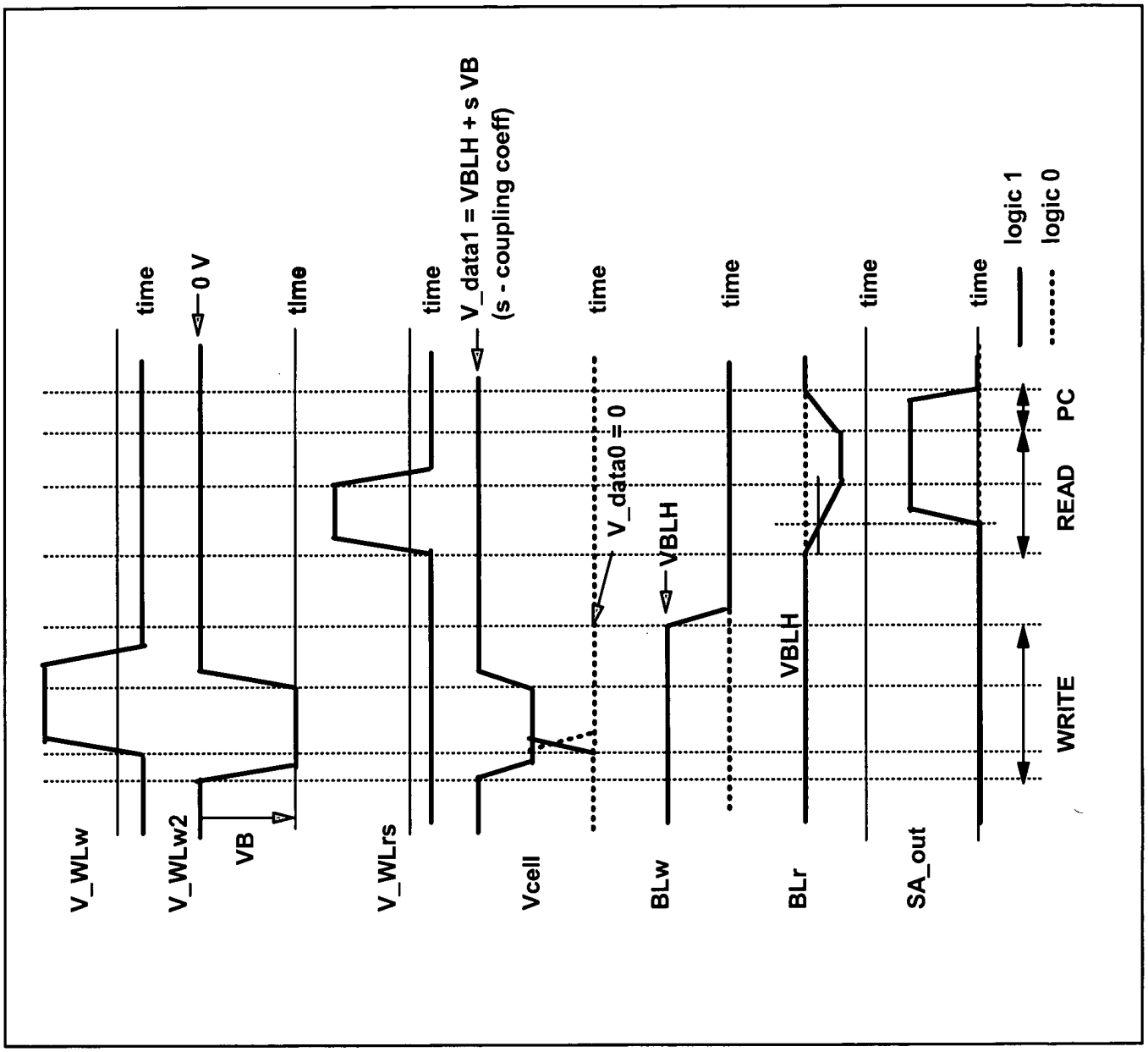

V_WLw
V_WLw2
VB
V_WLrs
Vcell
BLw
BLr
SA_out
time
0 V
V_data1 = VBLH + s VB
(s - coupling coeff)
V_data0 = 0
VBLH
logic 1
logic 0
READ
PC
WRITE

FIG. 18

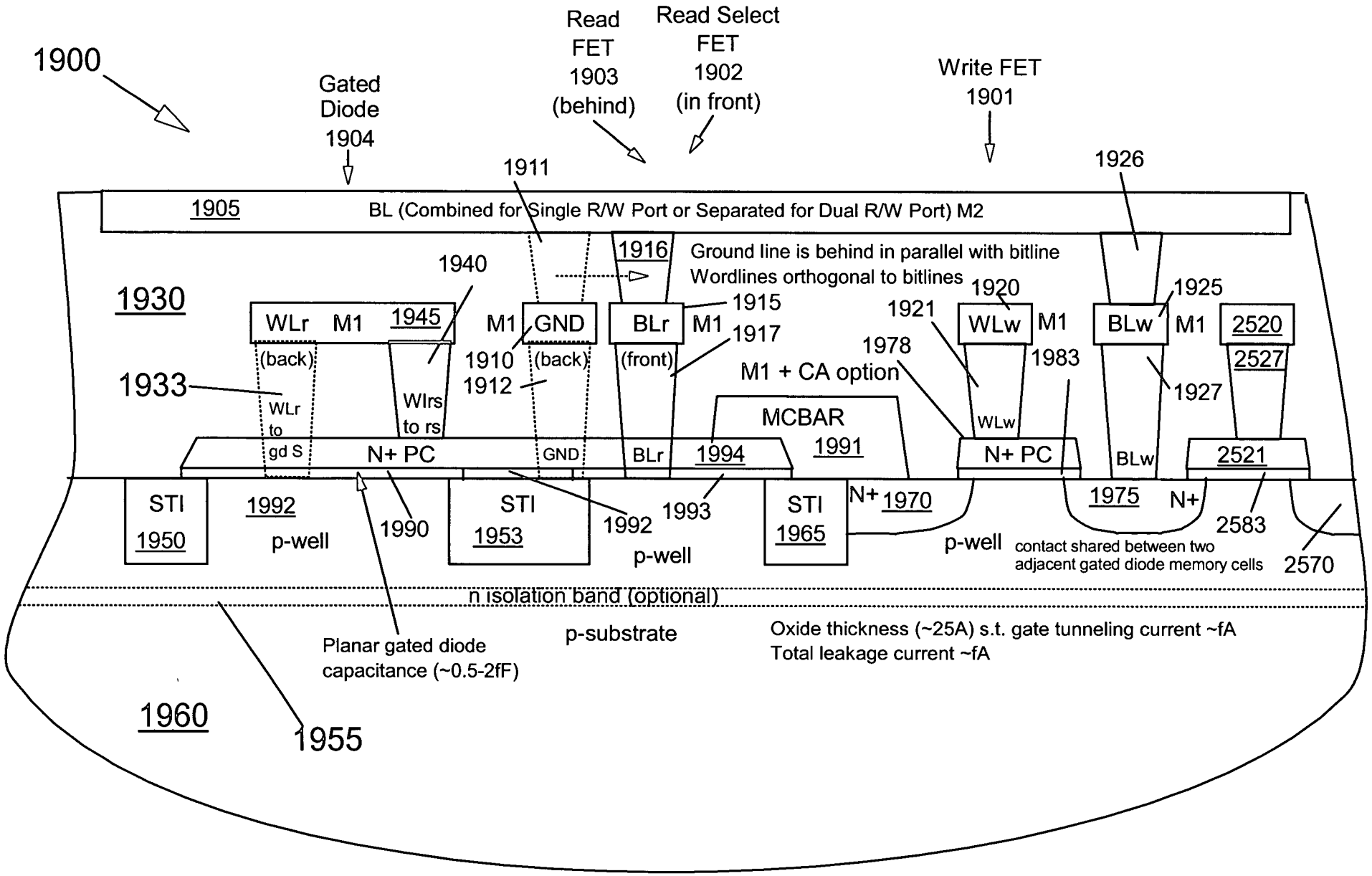

1900
Gated Diode 1904
Read FET 1903 (behind)
Read Select FET 1902 (in front)
Write FET 1901
1911
1926
1905
BL (Combined for Single R/W Port or Separated for Dual R/W Port) M2
1916
Ground line is behind in parallel with bitline
Wordlines orthogonal to bitlines
1940
1930
1920
1925
1915
1921
1917
1978
1983
1933
1910
1912
M1 + CA option
1927
MCBAR
1991
WLr to gd S
WIrs to rs
WLr M1 1945
M1 GND
BLr M1
WLw M1
BLw M1
2520
2527
(back)
(back)
(front)
WLw
BLw
N+ PC
GND
BLr
1994
N+ PC
2521
STI 1950
1992
p-well
1990
STI 1953
1992
1993
STI 1965
N+ 1970
1975
N+
2583
p-well
contact shared between two adjacent gated diode memory cells
2570
n isolation band (optional)
p-substrate
Oxide thickness (~25A) s.t. gate tunneling current ~fA
Total leakage current ~fA
Planar gated diode capacitance (~0.5-2fF)
1960
1955

FIG. 19

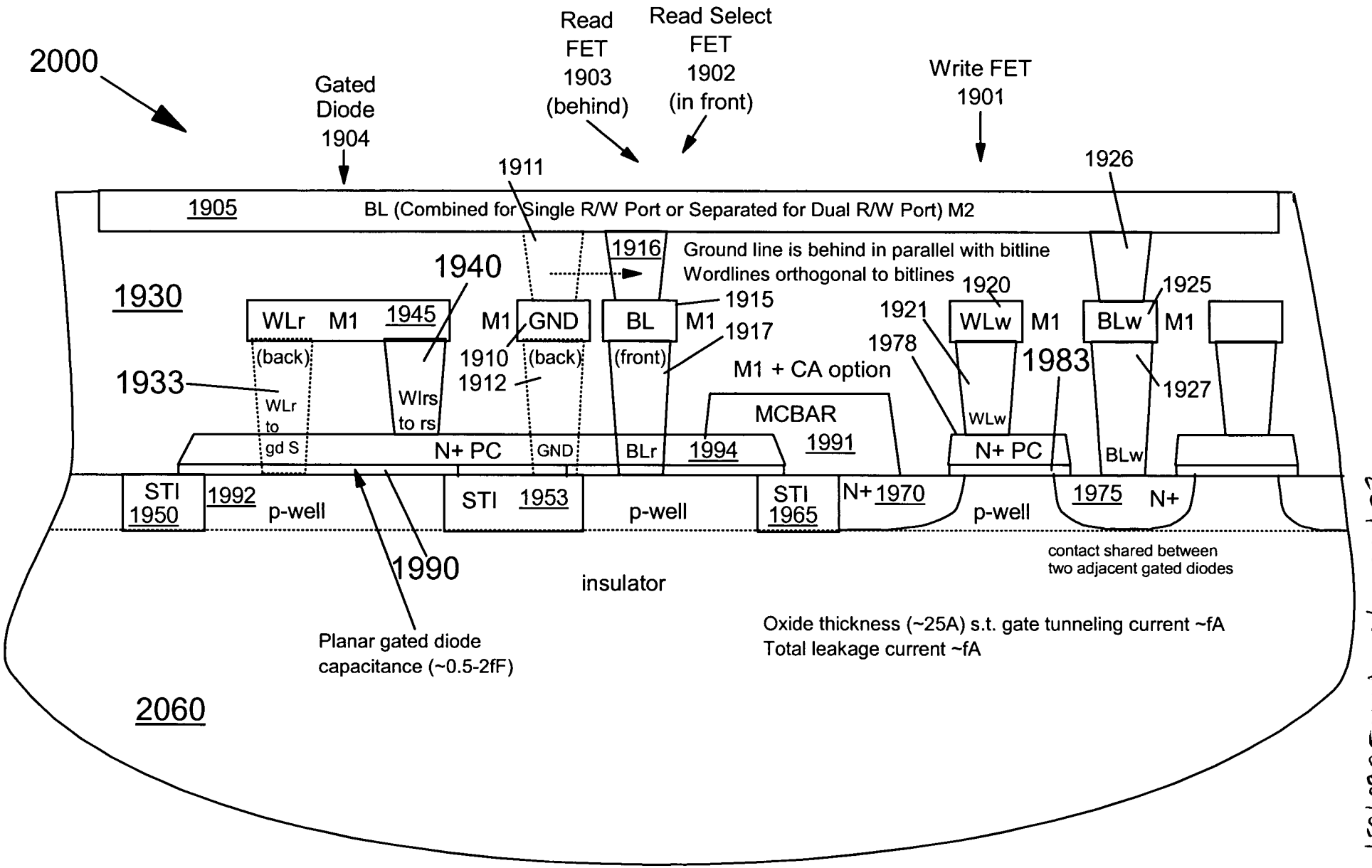

2000
Gated Diode 1904
Read FET 1903 (behind)
Read Select FET 1902 (in front)
Write FET 1901
1911
1926
1905
BL (Combined for Single R/W Port or Separated for Dual R/W Port) M2
1916
Ground line is behind in parallel with bitline
Wordlines orthogonal to bitlines
1940
1930
1920
1925
1915
1921
WLr M1 1945
M1 GND
BL M1
WLw M1
BLw M1
1917
1978
1910
1912
(back)
(back)
(front)
M1 + CA option
1983
1933
1927
WLr to gd S
WIrs to rs
MCBAR
WLw
1991
N+ PC
GND
BLr
1994
N+ PC
BLw
STI 1950
1992
p-well
STI 1953
p-well
STI 1965
N+ 1970
p-well
1975
N+
contact shared between two adjacent gated diodes
1990
insulator
Planar gated diode capacitance (~0.5-2fF)
Oxide thickness (~25A) s.t. gate tunneling current ~fA
Total leakage current ~fA
2060

FIG. 20

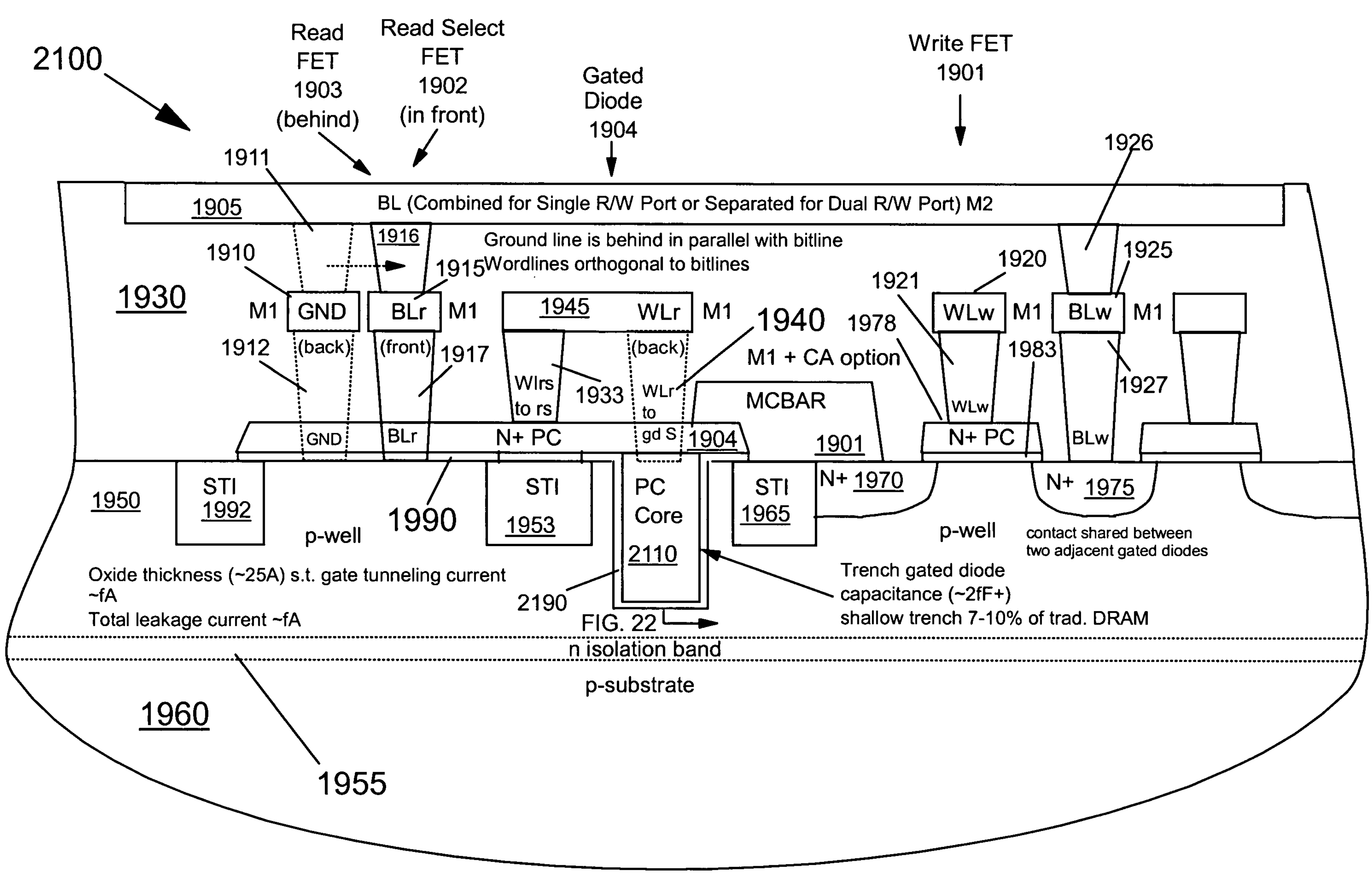

2100
Read FET 1903 (behind)
Read Select FET 1902 (in front)
Gated Diode 1904
Write FET 1901
1911
1926
1905
BL (Combined for Single R/W Port or Separated for Dual R/W Port) M2
1916
Ground line is behind in parallel with bitline
Wordlines orthogonal to bitlines
1910
1915
1920
1925
1921
1930
M1
GND
BLr
1945
WLr
1940
1978
WLw
BLw
1912
(back)
(front)
1917
M1 + CA option
1983
Wlrs to rs
1933
WLr to gd S
MCBAR
1927
GND
N+ PC
1904
1901
N+ PC
BLw
STI 1992
STI 1953
PC Core 2110
STI 1965
N+ 1970
N+ 1975
1950
p-well
1990
p-well
contact shared between two adjacent gated diodes
Oxide thickness (~25A) s.t. gate tunneling current ~fA
Total leakage current ~fA
2190
Trench gated diode capacitance (~2fF+) shallow trench 7-10% of trad. DRAM
FIG. 22
n isolation band
p-substrate
1960
1955

FIG. 21

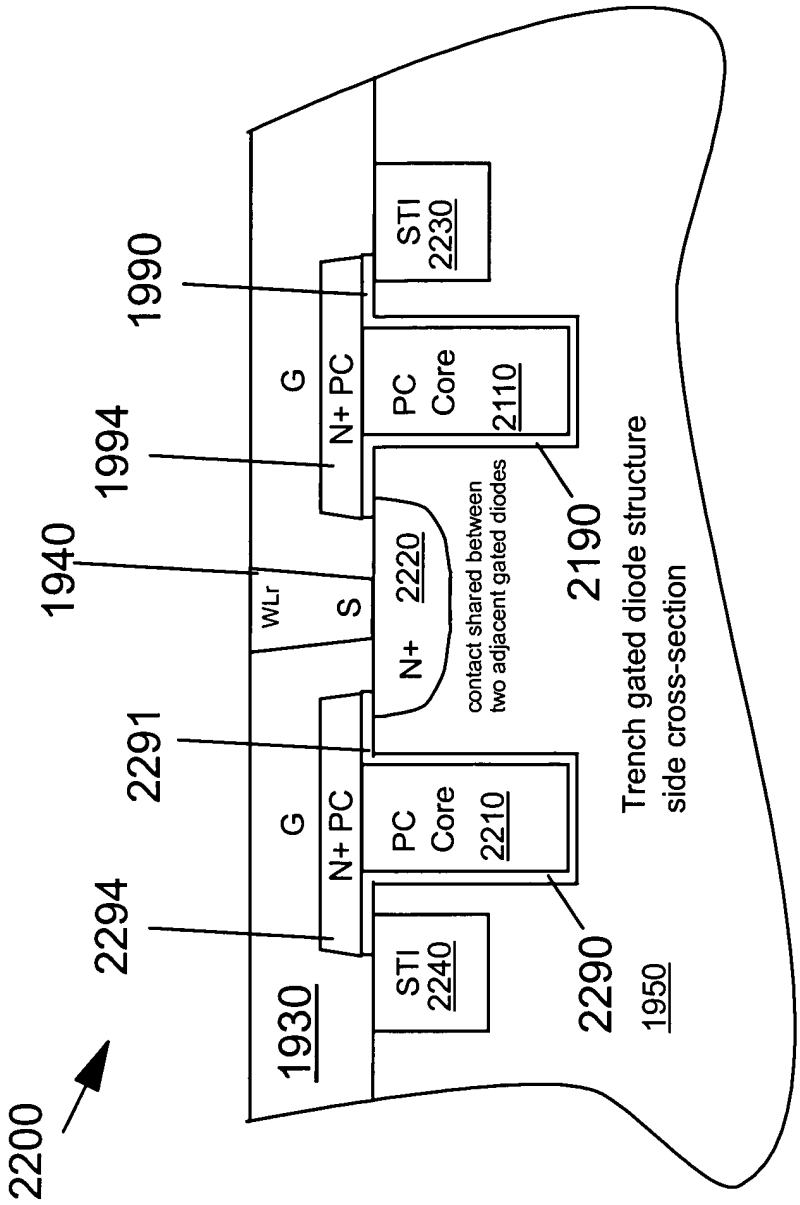

2200
1930
2294
2291
1940
1994
1990
STI 2240
N+ PC
G
PC Core 2210
N+ 2220
WLr
S
PC Core 2110
N+ PC
G
STI 2230
2290
2190
contact shared between two adjacent gated diodes
Trench gated diode structure side cross-section
1950

FIG. 22

1/OR9200306040051

FIG. 23

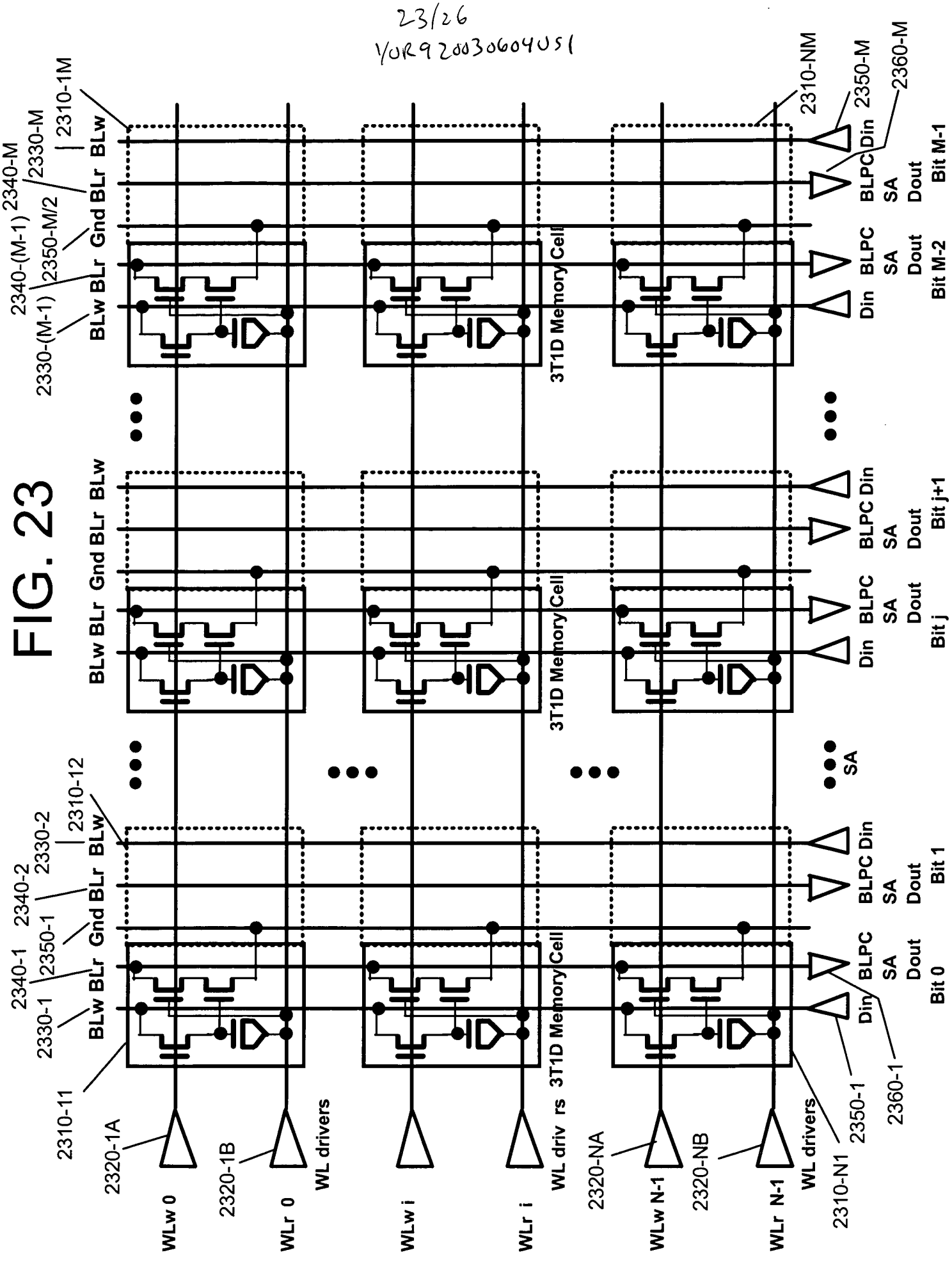
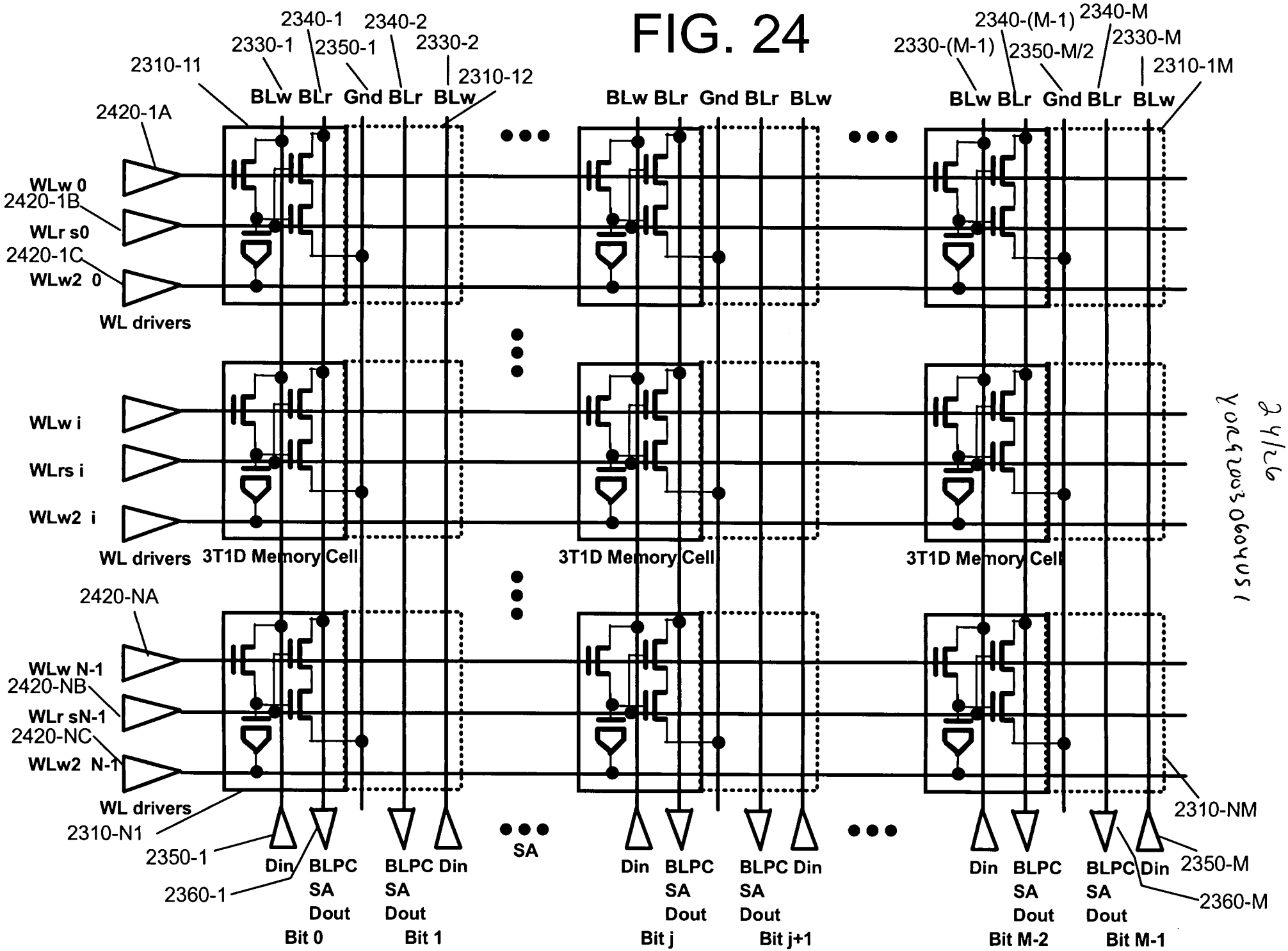


FIG. 24


2340-1
2340-2
2330-1
2350-1
2330-2
2310-11
2310-12
BLw BLr Gnd BLr BLw
2340-(M-1)
2340-M
2330-(M-1)
2350-M/2
2330-M
2310-1M
2420-1A
WLw 0
2420-1B
WLr s0
2420-1C
WLw2 0
WL drivers
WLw i
WLrs i
WLw2 i
3T1D Memory Cell
2420-NA
WLw N-1
2420-NB
WLr sN-1
2420-NC
WLw2 N-1
2310-N1
2350-1
2360-1
Din
BLPC
SA
Dout
Bit 0
Bit 1
Bit j
Bit j+1
Bit M-2
Bit M-1
2310-NM
2350-M
2360-M

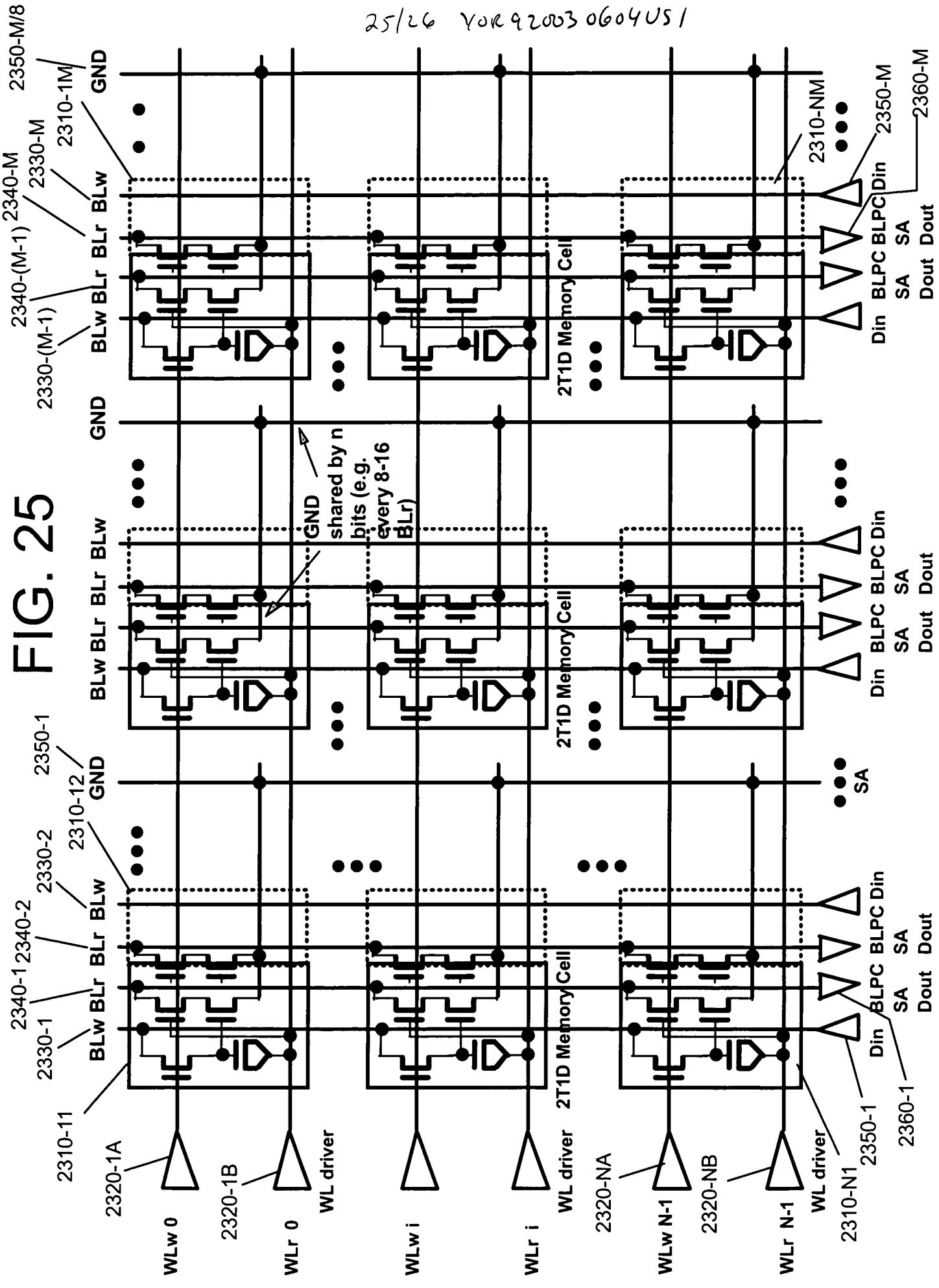

2350-M/8
2350-M
2360-M
2340-M
2330-M
2310-1M
2310-NM
2340-(M-1)
2330-(M-1)
GND
BLw BLr
2T1D Memory Cell
Din BLPC
SA
Dout
Bit M-1
Bit M-2
GND shared by n bits (e.g. every 8-16 BLr)
Bit j
Bit j+1
2350-1
2360-1
2340-2
2330-2
2310-12
2340-1
2330-1
2310-11
2320-1A
2320-1B
2320-NA
2320-NB
2310-N1
WL driver
WLw 0
WLr 0
WLw i
WLr i
WLw N-1
WLr N-1
Bit 0
Bit 1

FIG. 25

FIG. 26